REMARKS

A. Request for reconsideration

Applicants have carefully considered the matters raised by the Examiner in the Office Action but remains of the position that patentable subject matter is present. Applicant respectfully requests reconsideration of the Examiner's position based on the Claim Amendments and following remarks.

B. Request for One-month Extension of Time

Applicants respectfully request one month extension of time to answer the outstanding Office Action. The extension fee is concurrently paid with this online filing.

C. Claim Status and Amendments

Claims 1-8 and 25-27 are presented for further prosecution. Claims 9-24 have been cancelled. Claims 26 and 27 have been added.

Claims 1 and 2 have been amended to more particularly point out the corporate effect comes from a current parallel to a surface of the MFC and a part of the current

branched vertically through the MFC. Support for these amendments can be seen, for example, from the 2nd paragraph on page 6 of the application as filed, in particular, from lines 15-17 of page 6.

New claims 26 and 27 mirror the claims 1 and 2. They are added to explicitly recite 1) a part of the parallel current being branched vertically through the MFC in the method claim; and 2) a current-limiting mechanism to branch out a part of the parallel current to flow vertically through the MFC in the product claim. Support for these new limitations can be seen, for example, at the 2nd paragraph of page 6 and the 2nd paragraph of page 7.

No new matter is added by the amendments.

D. Prior Art Rejections under 35 USC §102

The Examiner takes the position that all the claims are anticipated by Nakamura under 35 USC §102.

In order to maintain an anticipation rejection under 35 U.S.C. § 102, the prior art must disclose each and every element of the rejected claims with sufficient clarity to prove its existence in the prior art. Applicants

respectfully submit that Nakamura does not anticipate claims 1-8 and 25-27.

1. Nakamura does not teach a control method utilizing the corporate effect of a parallel current and a branching out vertical current, as in Claim 1 and its dependent claims.

Nakamura et al discloses a dual-barrier magnetic cell for which the "writing operation" is performed by passing the current I (column 6 lines 26-column 7 lines 65, also Seen in the figures of Nakamura) across the interfaces, which is perpendicular to the surface of the MFC. Clearly, Nakamura does not teach or suggest using the magnetic effect generated by the current parallel to the surface of the MFC and branching a part of the same current vertically to the surface of MFC to perform the writing-in operation.

As shown in FIG. 4 of the present invention, when the current is large, there are two currents vertical to each other: Current I_1 being parallel to the surface of the magnetic film cell MFC and Current I_2 being vertical to the surface of the magnetic film cell MFC. Fig. 5 indicates the magnetic fields generated by these currents in the free layer of the magnetic film cell MFC. The magnetic field

generated by current I_1 is in the easy magnetization axis direction of the magnetic film cell MFC, and the magnetic field generated by the current I_2 is a circular magnetic field within the free layer surface of the magnetic film cell MFC. Under the corporate effect of these magnetic fields, the magnetization reversion of the magnetic film cell MFC for the writing of information in the MRAM can be effectively implemented.

Nakamura is an old art. In Nakamura's writing operation, only the "spin-torque" effect of the current passing through the MFC is used. Nakamura has the problem that the current density passing through the MFC has to be a very large value and the large current density tends to cause overheating of the device and may burn it. This problem has been discussed in *Current-induced magnetization switching in a microscale ring-shaped magnetic tunnel junction*, Wei, H. X., M. C. Hickey, et al. Phys. Rev. B 77, 132401 (2008). See attached.

The present invention solved that problem. It utilizes both the magnetic effect and spin-torque effect of the electrons from the same current. The present invention uses both a reversion magnetic field generated by a current

parallel to the surface plane of a memory cell and a circular magnetic field generated by a current vertical to the surface plane of the memory cell. Therefore the present invention reduces the current passing through the device and decreases the risk of burning-out.

2. Nakamura does not teach a MRAM with the structure for the corporate effect of the parallel current and the branching out vertical current, as in Claim 2 and its dependent claims.

The present invention as in Claim 2 provides a MRAM with the configuration utilizing both the magnetic effects generated by a current parallel to the surface of the MFC and a current vertical to the surface of the MFC. In contrast, Nakamura's dual-barrier magnetic cell has no structure for the current on the bit line parallel to the surface of the MFC to be branched vertically through the MFC.

As shown in FIG. 3, the present invention provides MRAM unit 1 comprises a magnetic film cell MFC 2, a transistor ATR 4, a transitional metal layer 3b, contact holes 3e and 3f and a bit line BL 3a, a word line WL 3d and ground line GND 3c. The magnetic film cell MFC 2 is

arranged under the bit line BL 3a and its upper electrode is connected directly to the bit line BL 3a. The lower electrode of the magnetic film cell MFC 2 is connected to the transistor ATR 4 through the transitional metal layer 3b and the contact hole 3f. In the writing operation, the configuration of the MRAM device in the present invention provides a corporate magnetic field will result in magnetization reversion of the magnetic film cell MFC to achieve the writing of the data.

E. Regarding the New Claims 26 and 27

New claims 26 and 27 explicitly recite the current-limiting mechanism in the method and in the device, which is not disclosed in the cited references.

As discussed at the 2nd paragraph on Page 6, in order to branch out an appropriate part of a current on the bit line BL 3a to flow vertically to the ground GND 3c during a writing operation, one or more current-limiting mechanisms is arranged on each bit line BL of the MRAM array. The current-limiting mechanism is integrated in a peripheral circuit of the MRAM array and can be composed by diodes and transistors.

In the writing operation, the writing current is introduced into the bit lines, which is parallel to the selected magnetic film cell MFC 2. By the current-limiting mechanism, the current on the bit line will flow through the magnetic film cell MFC 2 to GND 3c.

In summary, no cited reference teaches a distinctive feature of the present invention as claimed in claims 1-8 and 25-27, which is the corporate effect created from concurrent use of a current parallel to the MFC and a part of the current being introduced vertically through the MFC. This feature reduces the number of lines and number of the metal wiring layers and the contact holes in the MRAM device, thus greatly reduces the complexity of MRAM's structure, and decreased the difficulty and the cost of manufacturing the device.

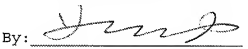
It is therefore respectfully submitted that Nakamura does not teach the corporative feature in the present invention with sufficient clarity, and the anticipation rejections based on Nakamura can not be maintained. The invention as claimed is patentable over the cited references taken alone or in combination.

F. Conclusion

In view of the foregoing and attached, it is respectfully submitted that the application is in condition for allowance and such action is respectfully requested. Should any further fees or extensions of time be necessary in order to maintain this Application in pending condition, appropriate requests are hereby made and authorization is given to debit Account # 02-2275.

Respectfully submitted,

LUCAS & MERCANTI, LLP

By: 

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